PVMC Tackles c-Si Metrology Challenges

Kristopher Davis, Hubert Seigneur, Andrew Rudack, Winston V. Schoenfeld
U.S. Photovoltaic Manufacturing Consortium (PVMC)

Abstract

The crystalline silicon (c-Si) activities of the U.S. Photovoltaic Manufacturing Consortium (PVMC), headquartered in New York,[1] have gone through a Pareto exercise with 38 separate organizations from the industry, national labs and academia to identify and prioritize the critical challenges in c-Si metrology. These challenges are organized into four different production areas: feedstock and wafer production; cell production; module production; and cross-cutting, i.e., multiple production areas. Identifying the most significant c-Si metrology hurdles is the first step in initializing collaborative R&D consortium projects that will spur U.S. industry progress in c-Si metrology solutions.

Introduction to PVMC

The U.S. Photovoltaic Manufacturing Consortium (PVMC) is a partnership led by SEMATECH and the College of Nanoscale Science and Engineering (CNSE) of the University at Albany. PVMC is an industry-led consortium for cooperative R&D among industry, university and government partners to accelerate the development, commercialization and manufacturing of solar photovoltaic (PV) systems.

Consortium activities include identifying and undertaking collaborative research projects, developing standards, drafting technology roadmaps and fostering increased connectivity among U.S. manufacturers. PVMC was created as part of the U.S. Department of Energy's (DOE) SunShot initiative.[2] The two PV technologies it is currently addressing include CIGS and c-Si. The c-Si branch activities are conducted at the University of Central Florida (UCF), with two initial c-Si program areas: (1) feedstock/wafer and (2) metrology.

PVMC c-Si Metrology Program

The c-Si Metrology program covers the breadth of the entire c-Si supply chain: not only wafers, cells and modules, but process gases for polysilicon production, pastes for cell metallization, module encapsulation materials and everything in between. Its scope furthermore includes a multitude of offline, in-line and *in situ* measurement and inspection techniques, such as the following:

- Materials characterization[3]
  - Electron microscopy
  - Surface characterization
  - Elemental/chemical composition analysis
- Wafer and cell analysis[4]
  - Optical and electrical properties
  - Mechanical/thermomechanical properties
  - Spatially resolved defect characterization[5]
- Cell and module performance[6]
  - *I-V* characteristics
  - Quantum efficiency, spectral response
- Module reliability/durability[7]
  - Failure mode identification
  - Energy yield over time, degradation rate quantification

c-Si Metrology Challenges List

Before selecting collaborative R&D projects for c-Si metrology, challenges in the c-Si metrology sector were scrutinized to ensure the projects would intersect with top industry challenges in c-Si metrology. Starting in December 2011, experts from the PV industry, academia, national labs and standards organizations were invited to identify c-Si metrology gaps throughout the entire c-Si PV value chain. Individuals from 59 separate entities provided input to this list, which was organized into four different production areas: (1) feedstock and wafer production; (2) cell production; (3) module production; and (4) cross-cutting, i.e., multiple, production areas.

In all, 44 c-Si metrology challenges were identified and subsequently ranked by representatives from 38 organizations using a simple voting mechanism and Pareto analysis (note: a similar listing/Pareto effort was undertaken for the c-Si PVMC Feedstock/Wafer program area, but these results are not included here).

Critical c-Si metrology challenges were defined as those that fell within the standard deviation (1σ) of the top score for that production area. Five such challenges were relegated to feedstock and wafer production, cell production and cross-cutting areas, and four to module production.

Pareto Analysis of c-Si Metrology Challenges

Code	Feedstock & Wafer Production Metrology Challenges
FW-C1	High-speed evaluation of crystal structure/orientation (crystal structure and orientation for mono, grain size and orientation for multi)
FW-C2	Monitoring thermal loads during polysilicon production and crystal growth
FW-C3	Measuring physical dimensions of wafers (e.g., flatness, TTV)
FW-C4	**Carrier lifetime measurements (e.g., high-throughput single point, mapping, measurements on as-cut wafers, separating lifetime due to bulk vs. surface recombination)**
FW-C5	**High-speed/real-time identification of areas (ingot and wafer) with high defect density**
FW-C6	**Evaluating uniformity of wafers from different polysilicon sources, ingots, bricks, etc.**
FW-C7	**Early detection of precursors (defects, etc.) that lead to future wafer/cells cracks during processing; evaluating mechanical integrity of ingots and bricks to identify sources of cracked wafers and cells later during production**
FW-C8	**Reliable/repeatable "go/no-go" breakage test correlated to microcrack size, location, etc.**

Table 1 – Feedstock and Wafer Production Challenges (top 5 highlighted)

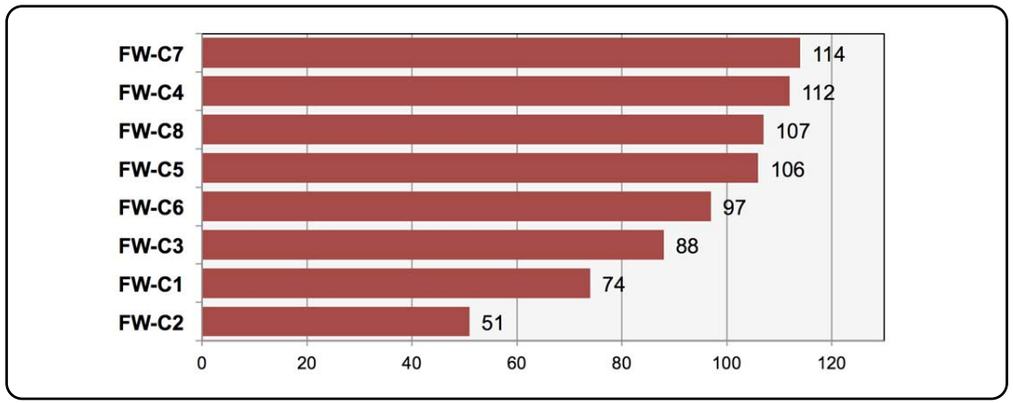

Figure 1 – Feedstock and Wafer Production Metrology Challenges/Pareto

Code	Cell Production Area Metrology Challenges
C-C1	**Evaluating mechanical integrity of standard and thin wafers/cells during cell processing (e.g., stress, presence of cracks, predicting cell breakage from stress/crack data); correlation between mechanical characteristics/properties of wafer and breakage during and after cell processing**
C-C2	**Electrical characterization of wafers and cells during cell processing (e.g., capacitive techniques, carrier lifetime, measuring J_0 for each cell component)**
C-C3	Characterization of surface roughness (e.g., determining morphology after cell texturing or saw damage removal, lack of standards)
C-C4	*In situ* monitoring of ARC/passivation layer deposition rate and thickness
C-C5	Measuring optical properties of surfaces and coatings (e.g., overcoming challenges caused by measuring textured surfaces, in-line reflectance measurements after texturing, reflectance at different angles of incidence, complex refractive index of ARC, in-line PL measurement)
C-C6	**Identifying and mapping defects at line speeds throughout cell manufacturing (e.g., locating shunts and hot spots using EL, PL, DLIT)**
C-C7	Evaluating passivation quality (e.g., grain boundary passivation for multi, passivation layers for mono and multi)
C-C8	Evaluating cell contacts (e.g., ensure organic binders are removed, ensure frit fired through completely and electrical contact has been formed, ensure proper adhesion, pinpointing components of series resistance, grid line resistance and line width measurement)
C-C9	**Advanced cell performance measurements (e.g., in-line QE, I-V as a function of angle of incidence and temperature, dark *I-V*, diode properties)**
C-C10	Automated inline or *In situ* monitoring of etch rate after/during texturing and chemical edge isolation
C-C11	High-throughput evaluation of emitter doping process (e.g., doping uniformity at the surface, resistivity mapping, in-line resistivity, junction depth, measuring doping profile on a textured surface)
C-C12	**Wafer and cell handling during measurements (standard thickness and thin wafers); thin wafer metrology compatibility and handling, non-contact methods**
C-C13	Double-sided metrology measurements on a linear track

Table 2 – Cell Production Challenges (top 5 highlighted)

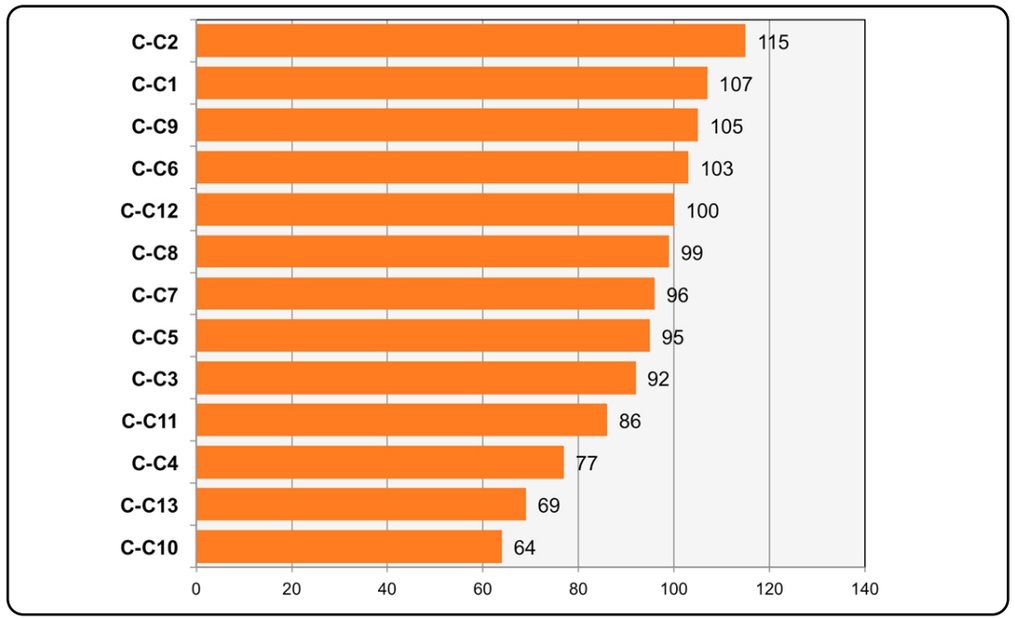

Figure 2 – Cell Production Metrology Challenges/Pareto

Code	Module Production Metrology Challenges
M-C1	Optical characterization of module materials (e.g., glass, encapsulation)
M-C2	*In situ* monitoring of the heat applied during cell interconnection
M-C3	**Mechanical characterization of cell interconnects (e.g., stress-strain of tabbing ribbons, solder bond quality, impact of tabbing on cells); Predicting solderability of the cells and ribbons (e.g., lack of standards or metrics to properly evaluate)**
M-C4	*In situ* monitoring of polymer cross-linking during lamination; Measuring interfacial adhesion of polymeric materials
M-C5	**Advanced module performance measurements (e.g., spectral response, series and shunt resistance, I-V characteristics as a function of angle of incidence, temperature and irradiance)**
M-C6	Modeling/correlating energy yield (kWh/kW) for various climate zones using data measured at the factory floor (e.g., I-V under varying conditions, spectral response); Study of unknown effects on energy yield such as soiling
M-C7	Evaluation of module safety (e.g., insulation quality, frame continuity, mechanical integrity)
M-C8	**Identification of failure modes in the factory before being shipped (e.g., locating hot spots, cracks in module glass)**
M-C9	Improved standardized test methods for testing reliability of components and subcomponents (e.g., accelerated aging, bypass diode evaluation, effect of soiling)
M-C10	**Identifying/locating defects induced during module manufacturing from start to finish**

Table 3 – Module Production Metrology Challenges (top 4 highlighted)

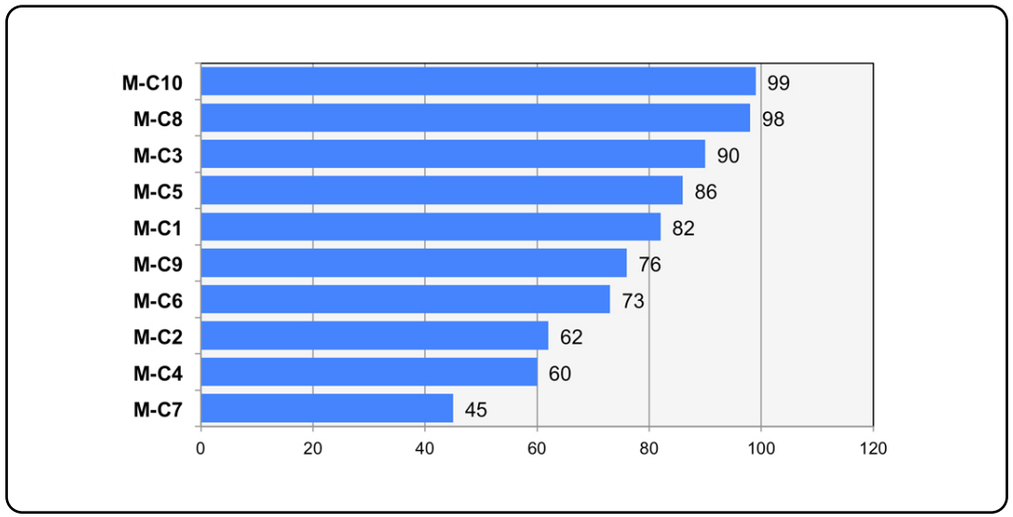

Figure 3 – Module Production Metrology Challenges/Pareto

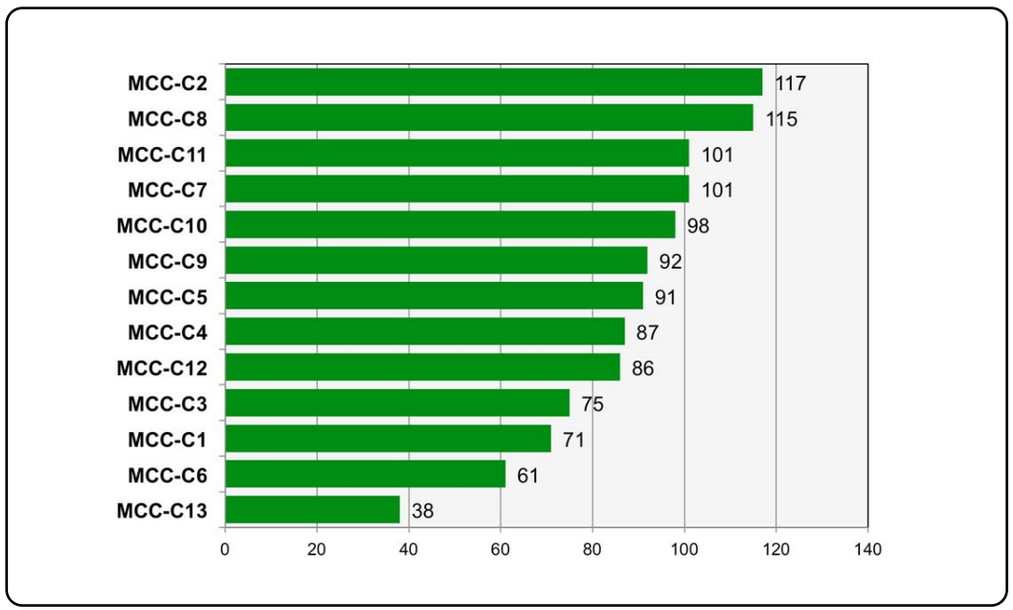

Figure 4 – Cross-cutting Metrology Challenges/Pareto

Code	Cross-Cutting Metrology Challenges
MCC-C1	Evaluating the quality of process gases, chemicals, polymers, pastes/inks and other key manufacturing materials (e.g., *in situ*, spot checking); Trace impurity detection of bulk materials and surfaces (e.g., cross-sectional electron microscopy, depth profiling)
MCC-C2	**Integration standards: Integration of in-line and *in situ* metrology into process control (e.g., lack of standardized format for data output, compatibility of data with manufacturing software, added cost of data customization); Lack of unified standards for integrating in-line metrology hardware into manufacturing lines (e.g., size, throughput, handling)**
MCC-C3	Process simulation and cell/module performance modeling tools/techniques
MCC-C4	Correlation of different metrology techniques that measure the same parameter (benchmarking)
MCC-C5	Imaging-based automated inspection methods for cell and module manufacturing (e.g., alignment and aspect ratio of front-grid contacts, color uniformity, straight conductor lines for modules)
MCC-C6	Lack of knowledgeable and properly trained workforce
MCC-C7	**Commercialization of existing metrology techniques (e.g., demonstration on actual production lines, ROI determination, achieving higher throughput); Establishing value (ROI) of collecting more data in manufacturing**
MCC-C8	**Correlation of cell and module metrology data to module performance, efficiency and reliability (e.g., wafer quality/purity, defect presence, carrier lifetime mapping, shunt locations, optical properties of encapsulation, ARC refractive index, hot spot locations, presence of cracks, stress induced during tabbing, killer defects vs. tolerable defects)**
MCC-C9	Lack of communication of industry needs from cell/module manufacturers to metrology tool suppliers; Better open knowledge of the needs and trends for metrology to guide product development; Lack of samples (wafers, cells, modules) available for metrology vendors to test and evaluate their tools/techniques
MCC-C10	**Value-cost curve for metrology tools (e.g., determining optimal sampling rates, scan densities, accuracy and throughput that provides the most value at a reasonable cost); Determining relative priority of all measurement techniques**
MCC-C11	**Wafer/cell identification, and tracking and traceability from source materials to final product (e.g., horizontal communication of metrology data from start to finish, tracking defects)**
MCC-C12	Process control software to provide cross-cut tracking of performance using wafer, cell and module metrology data as well as providing quality control for precursor materials and relating process parameters to cell/module performance; fault detection and classification software
MCC-C13	Demonstrate relationship of electrostatic control and measurement to process-induced defectivity

Table 4 – Cross-Cutting Metrology Challenges (top 5 are highlighted)

Summary

The c-Si activities of the U.S. PVMC has assembled a comprehensive list of industry challenges in c-Si PV metrology and carried out a Pareto ranking exercise to identify the top gaps within four production area categories. Given the dynamic nature of the PV market, the identification and ranking of challenges is expected to be an annual PVMC activity to ensure results align with current industry challenges. The next step is to formulate meaningful, high-impact, pre-competitive consortium projects to address the challenges. These potential c-Si metrology projects will likewise undergo similar Pareto ranking to identify top projects that will be vetted by the Metrology Technical Advisory Board for final selection. In conclusion, the U.S. PV c-Si metrology sector

has many challenges moving ahead, but is poised to tackle them through an industry-led R&D consortium.

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About the Authors

Kristopher Davis *is currently the program manager for c-Si Metrology projects at PVMC in Orlando, Florida. He has a B.S. in electrical engineering and an M.S. in optics & photonics, both from UCF. Since 2007, he has been working on R&D in photovoltaics at the Florida Solar Energy Center, a research institute of UCF.*

Hubert Seigneur *is currently the program manager for c-Si feedstock/wafer projects at PVMC in Orlando, Florida. He earned his B.S. in computer engineering, his M.S. in electrical engineering and his Ph.D. in optics & photonics, all from the University of Central Florida. Before joining the PVMC, he was a postdoctoral fellow at the Florida Solar Energy Center.*

Andrew Rudack *is a SEMATECH assignee and Emerging Programs manager at PVMC in Orlando, Florida. He is a graduate of the Environmental Science program at the State University in Plattsburgh, New York, and a 33-year veteran of the semiconductor industry.*

Winston V. Schoenfeld *is currently director of c-Si PVMC operations in Orlando, Florida. He has a Ph.D. from UCSB, has held multiple positions in industry/academia and is a tenured faculty member at UCF, with more than 120 authored/co-authored publications.*