PVMC Tackles c-Si Feedstock and Wafering Challenges

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Abstract
The crystalline silicon (c-Si) program of the U.S. Photovoltaic Manufacturing Consortium (PVMC) performed a Pareto exercise with more than 30 separate organizations from industry, national labs, and academia to identify and prioritize the critical challenges for c-Si feedstock and wafering. An annual Pareto exercise such as this is not only a valuable tool to guide the identification and selection of potential consortium projects, but also an essential step towards achieving true consensus among its members. In addition to providing the results of this latest Pareto exercise, this article outlines the journey through the intricacies of this challenging yet exciting process.

Introduction to U.S. PVMC and c-Si Programs
The U.S. Photovoltaic Manufacturing Consortium (PVMC), headquartered in New York, is a partnership led by SEMATECH and the College of Nanoscale Science and Engineering (CNSE) of the University at Albany. PVMC is an industry-led endeavor for cooperative R&D among industry, university, and government partners to accelerate the development, commercialization, and manufacturing of solar photovoltaic (PV) systems in the U.S. [1]. PVMC's main mission is to accelerate the transition of new technologies into mainstream manufacturing. Consortium activities include engaging in collaborative research projects, developing standards, generating technology roadmaps, and fostering increased connectivity among U.S. manufacturers. PVMC was created in 2011 as part of the U.S. Department of Energy's (DOE) SunShot Initiative [2]. The two conversion technologies it currently addresses include copper indium gallium diselenide (CIGS) and crystalline silicon (c-Si).

The c-Si arm of PVMC is managed by the Florida Solar Energy Center, a research institute of the University of Central Florida in Orlando. PVMC has two initial c-Si program areas: (1) feedstock/wafering—the focus of this article—and (2) metrology, for which Pareto results were published previously [3]. The scope of the c-Si Feedstock and Wafering program covers the breadth of the entire feedstock, crystal growth, and wafering production areas including the following examples:

- Polysilicon Production
    - Electronic grade (EG)
        - Siemens process
        - Fluidized bed process
    - Solar Grade (SoG)
        - Elkem process
        - Direct carbothermic reduction process
        - Electrolysis process
- Crystal Growth
    - Monocrystalline Silicon

        - Czochralski (Cz) process
        - Floating zone (Fz) process
    - Multicrystalline Silicon
        - Block casting process
        - Bridgeman process
        - Gradient freeze process
    - Quasi-monocrystalline Silicon
- Wafering
    - Traditional
        - Slurry-based wire saw process
        - Diamond wire saw process
    - kerf-free
        - Implant-cleave process
        - Spalling process
        - Ribbon growth processes
    - Film c-Si deposition

PMVC Pareto Ranking Process

The Pareto exercise is a means to an end: the initiation of high impact research projects that will benefit consortium members and the U.S. PV industry as a whole. The entire process, which takes several months, is depicted in Figure 1. It consists of three steps: (1) identifying and ranking critical challenges, (2) identifying and ranking potential projects, and (3) selecting and initiating projects. This article addresses step 1, identifying critical challenges.

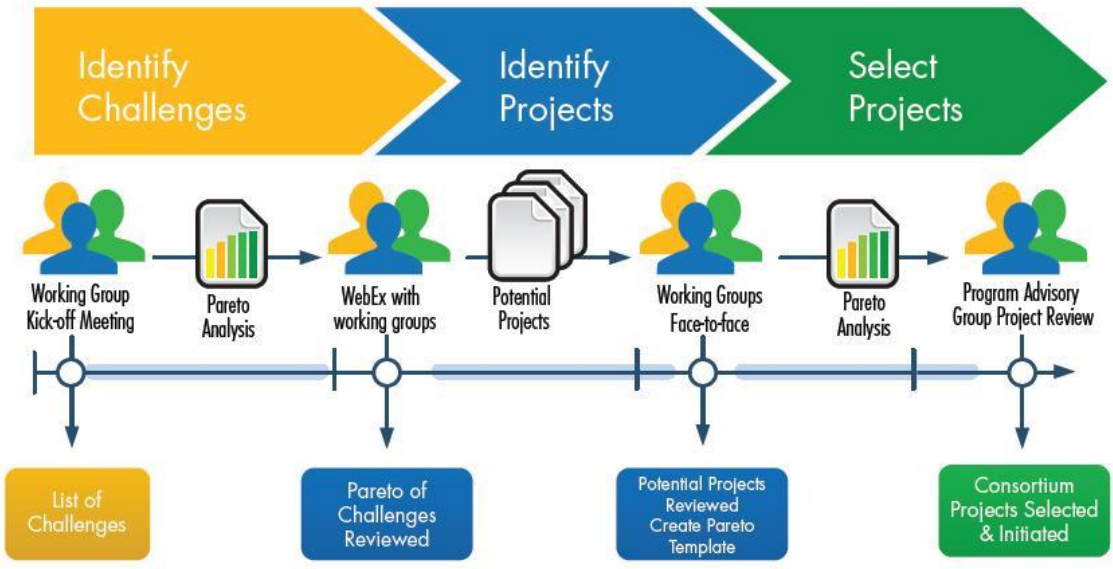

Figure 1 Process of Initializing Collaborative R&D Consortium Projects

Before beginning the ranking process, industry challenges in the feedstock and wafering sectors needed to be scrutinized. Starting in December 2011, invitations to participate in identifying c-Si feedstock and wafering challenges were issued to experts from the PV

industry, academia, national labs, and standards organizations. Individuals from 59 separate entities provided input to the list of challenges. In all, 36 c-Si feedstock and wafering issues were identified.

These issues were further divided into four different production areas: feedstock production, ingot production, wafer production, and "cross-cutting" or multiple production areas. Thirty-five representatives from 30 organizations then participated in ranking the challenges identified for each production area.

Code	Feedstock Production Area Challenges
F-C1	Lower polysilicon production cost and energy consumption (kWh/Wp)
F-C2	Gas recycling and reuse, byproducts
F-C3	7N or higher polysilicon
F-C4	Lack of unified/accepted materials standards; Having an accepted/standardized methodology for measuring all of the parameters that are important to identify feedstock quality
F-C5	Unestablished cell/module level reliability for non-EGS feedstock
F-C6	Understanding of relationship among feedstock quality/impurities/other parameters on resultant cell efficiency; Light-induced degradation as it relates to feedstock/wafer impurities; Differentiating killer impurities vs. impurities with minor impacts; Correlation of impurity measurements in polysilicon and resultant lifetime
F-C7	Crucible and crucible coating quality

Table 1 Feedstock Production Area Challenges

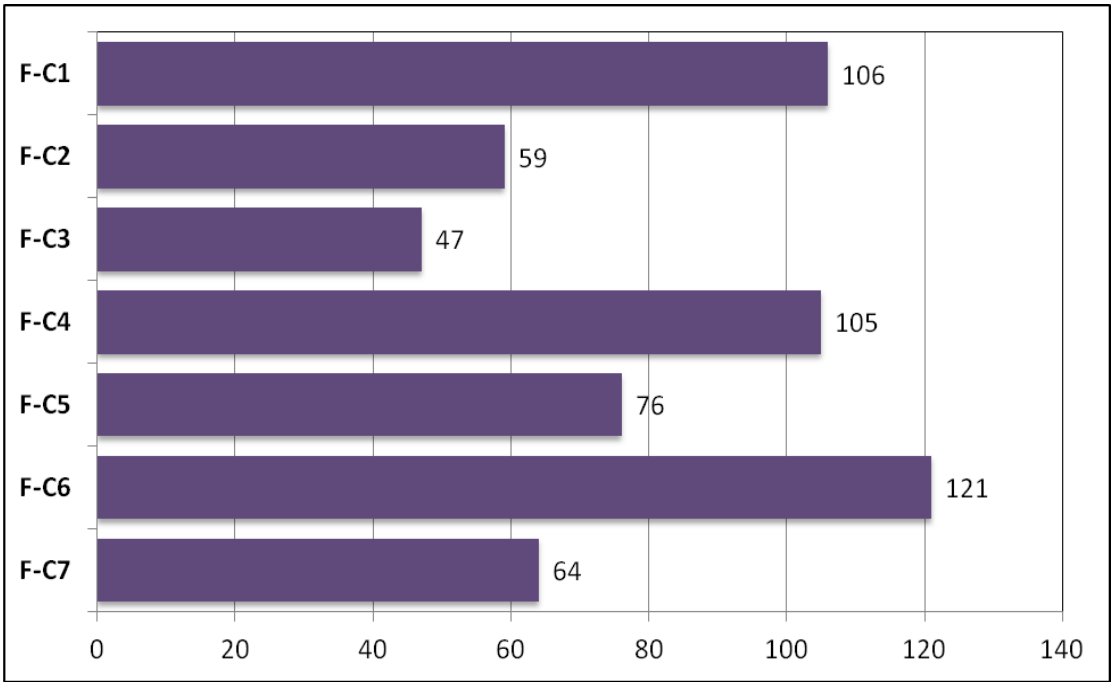

Figure 2 Pareto of Feedstock Production Area Challenges

Code	Ingot/Brick Production Area Challenges
IB-C1	Impurity control; Defect engineering techniques
IB-C2	Doping uniformity
IB-C3	Grain size control
IB-C4	Overall Si recycling, incorporating recovered Si back into crystal melt; Utilization and standardization of kerf fines for incorporation into melt
IB-C5	Characterization of compensated material (non-EGS)
IB-C6	Maintaining crystal quality while increasing mono ingot pulling rate/throughput
IB-C7	Superior furnace control… to produce superior ingots. Possible with fault detection and classification software, which correlates metrology data to tool trace data, enabling "golden" tool setpoints and alarms/corrective action when deviations occur

Table 2 Ingot/Brick Production Area Challenges

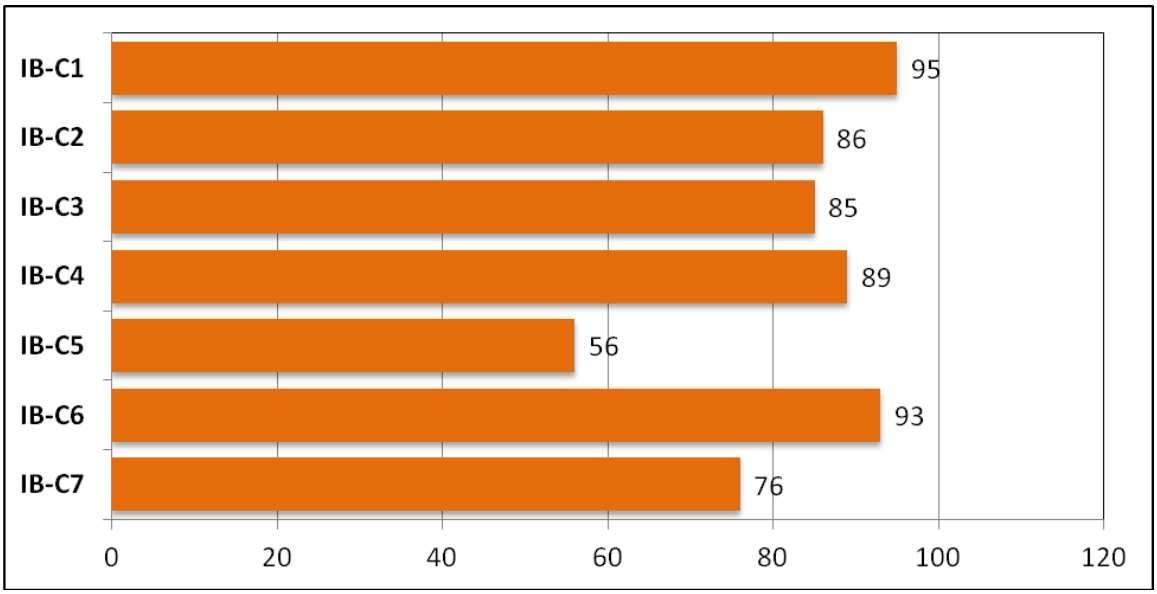

Figure 3 Pareto of Ingot/Brick Production Area Challenges

Code	Wafer Production Area Challenges
W-C01	Thin wafers handling and processing (e.g., limiting breakage); Thin wafer interconnection; Test methods or a specific handling target to characterize/validate handling for thin wafers; Pre-processing, handling, and packaging/shipment of thin wafers to cell manufacturer
W-C02	Slurry recycling
W-C03	Reduction of kerf loss
W-C04	Unified incoming wafer specifications and standards; Better specifications for mechanical and electrical characterization (affects cell efficiency & end product performance)
W-C05	Grain boundary passivation of multicrystalline Si wafers
W-C06	Determination of electrical activity of crystallographic defects in a wafer
W-C07	Understanding critical crack lengths vs. wafer thickness
W-C08	Wafer consistency
W-C09	Lack of detailed information from customers (only pass/fail info given); Lack of U.S.-based solar companies for partnerships

W-C10	Saw damage removal and surface characterization
W-C11	New wafering technologies (kerf-free, implant/cleave, direct wafer technology, etc.); Lower cost SOI wafers
W-C12	Correlation of reliability/degradation mechanisms to wafer quality/properties
W-C13	Decoupling bulk and surface recombination in carrier lifetime measurement; Carrier lifetime measurements at the wafer level, better prediction of cell efficiency
W-C14	Inline inspection of wafers; Determine optimal scan density and cost versus need (value-cost curve)
W-C15	Unknown impact of new wafer formats (e.g., quasi-mono wafers, n-type wafers, etc.) on cleaning and texturing processes

Table 3 Wafer Production Area Challenges

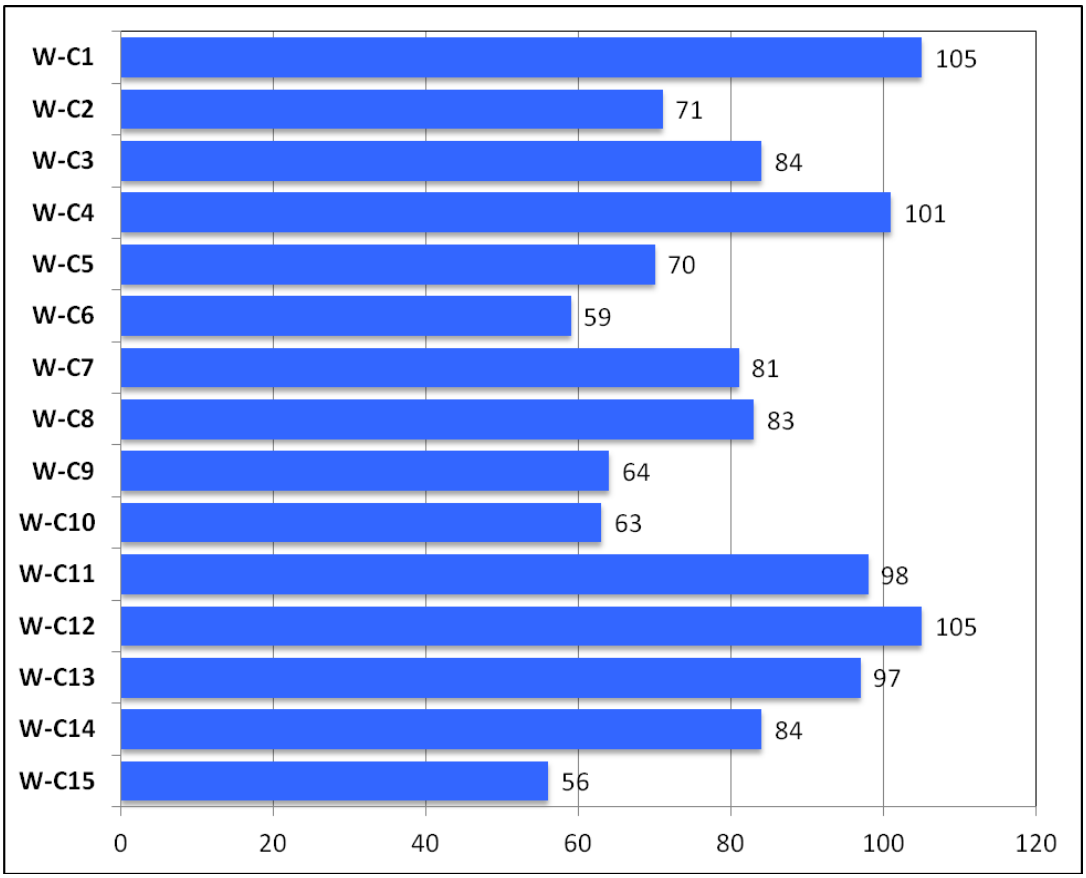

Figure 4 Pareto of Wafer Production Area Challenges

Code	Cross-cutting FS/W Production Area Challenges
FCC-C1	Equipment/factory automation, standardization (height, software, communications, etc.); Requirements for interface between handling systems and metrology tools
FCC-C2	Identifying, sharing, and establishing industry best practices through benchmarking
FCC-C3	Lack of knowledgeable and properly trained work force
FCC-C4	End-of-life Si recycling and reintroduction potential in feedstock/ingot formation
FCC-C5	Understanding uniformity and consistency of wafer quality from different feedstock sources, ingots, etc.
FCC-C6	Lack of knowledge/communication/acceptance of existing standards
FCC-C7	Demonstrate relationship of electrostatic control and measurement to process-induced defectivity

Table 4 Cross-Cutting FS/W Production Area Challenges

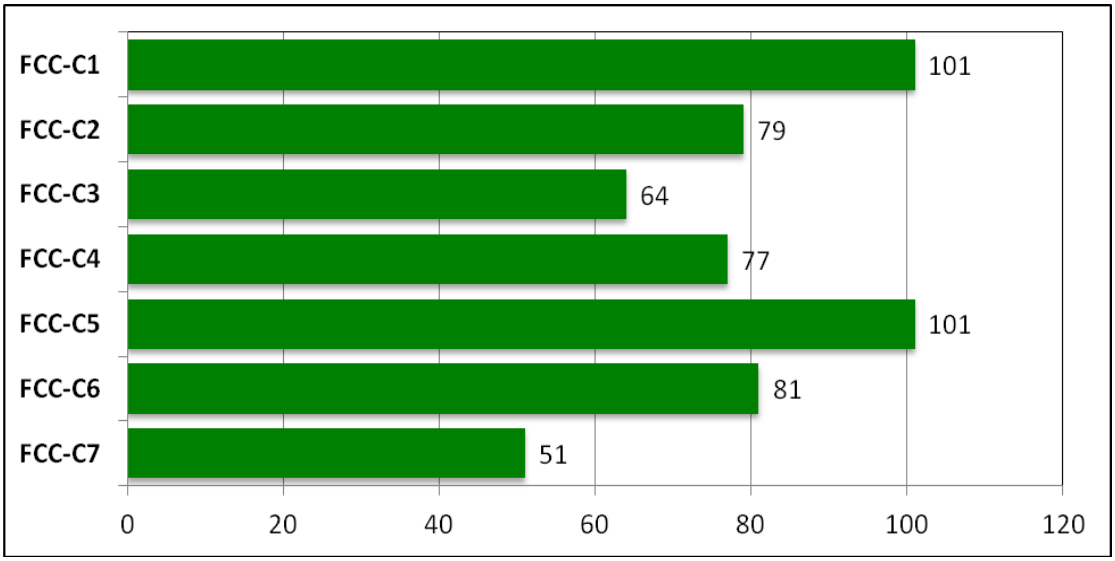

Figure 5 Pareto of Cross-Cutting FS/W Production Area Challenges

Summary

As a result of its Pareto ranking exercise, PVMC has compiled a comprehensive list of industry challenges in c-Si feedstock and wafering and identified the top challenges within four production area categories. Given the dynamic nature of the PV market, PVMC is likely to repeat this identification and ranking annually to ensure results align with current industry developments. The next step involved delineating meaningful, high impact, pre-competitive consortium projects to address the challenges. Potential projects then underwent a similar Pareto ranking exercise to identify top projects. PVMC is now at the last step of the process: review by the Program Advisory Group to ultimately select the projects the consortium will undertake. Although the U.S. PV feedstock and wafering sectors face many hurdles, PVMC is poised to tackle them.

References

1. www.uspvmc.org
2. http://www1.eere.energy.gov/solar/sunshot/index.html
3. K.O. Davis, H. Seigneur, A. Rudack, W.V. Schoenfeld, "PVMC Tackles c-Si Metrology Challenges," Future Photovoltaic, April 2012.

Biographies

Hubert P. Seigneur is currently the program manager for c-Si feedstock/wafering projects at PVMC in Orlando, Florida. He earned his bachelor's degree in Computer Engineering, his master's degree in Electrical Engineering, and his doctorate degree in Optics & Photonics, all from the University of Central Florida. Before joining the PVMC, he was a postdoctoral fellow and research scientist at the Florida Solar Energy Center.

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Andrew C. Rudack is a SEMATECH assignee and operations manager for c-Si Programs at PVMC in Orlando, Florida. He is a graduate of the Environmental Science program at the State University in Plattsburgh, New York, and a 33-year veteran of the semiconductor industry.

Winston V. Schoenfeld is currently Director of c-Si PVMC operations in Orlando, Florida. He has a Ph.D. from UCSB, has held multiple positions in industry/academia, is currently a division director at the Florida Solar Energy Center, and tenured faculty at UCF with more than 120 authored/co-authored publications.